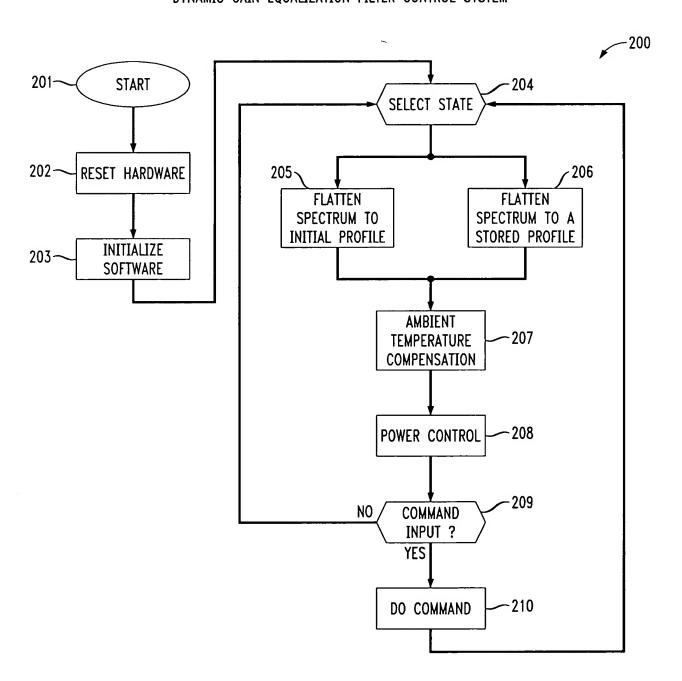


FIG. 1

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 $FIG.\ \mathcal{Z}$  Dynamic gain equalization filter control system

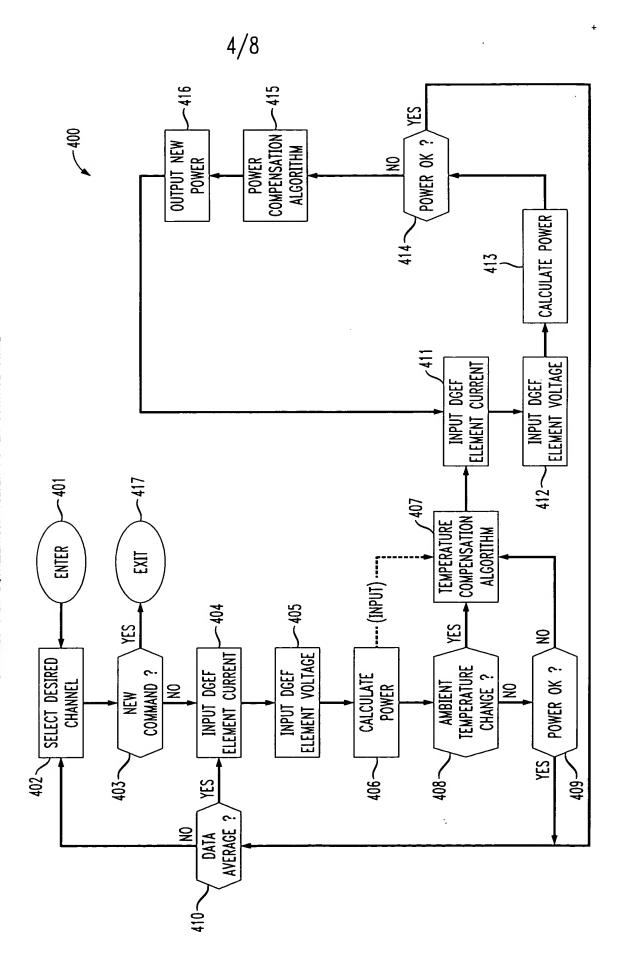


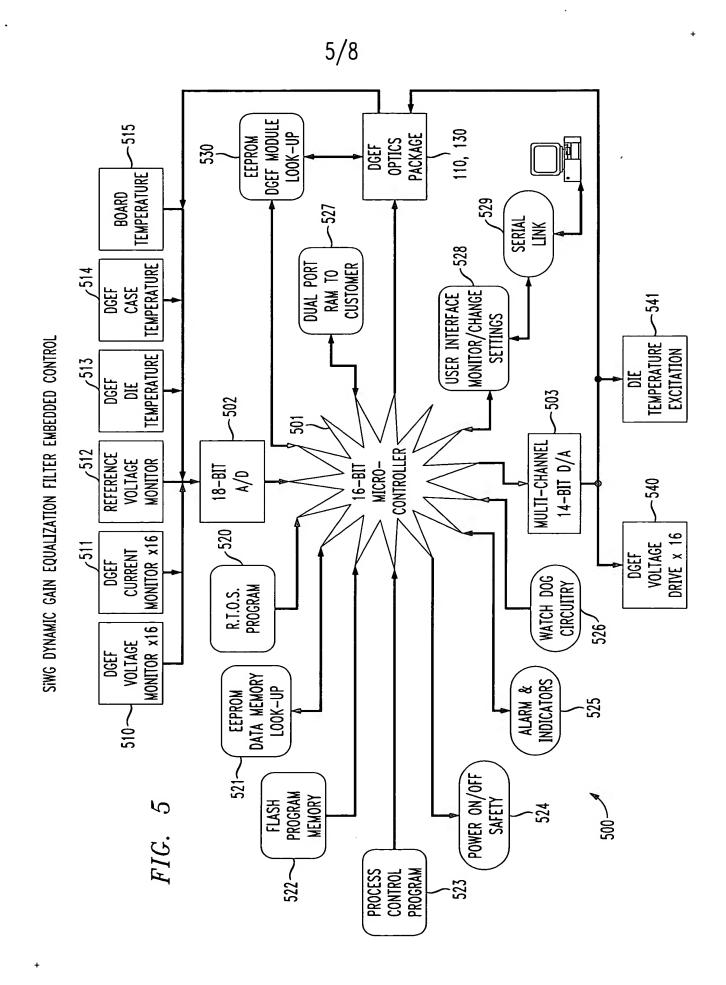
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-258 -259 .257 SET CUSTOMER PARAMETERS STORE ATTENUATION MEMORY TEST ERROR TEST REPORT 260~ DYNAMIC GAIN EQUALIZATION FILTER STATE DIAGRAM PROCESS COMMAND FIG. 3 <u>720</u> 254 .261 -252 HARDWARE COMMAND SET ATTENUATION SPECTRUM ~255 -253 HALT ON FAILURE -251 POWER CONTROL INITIALIZE

FIG. 4

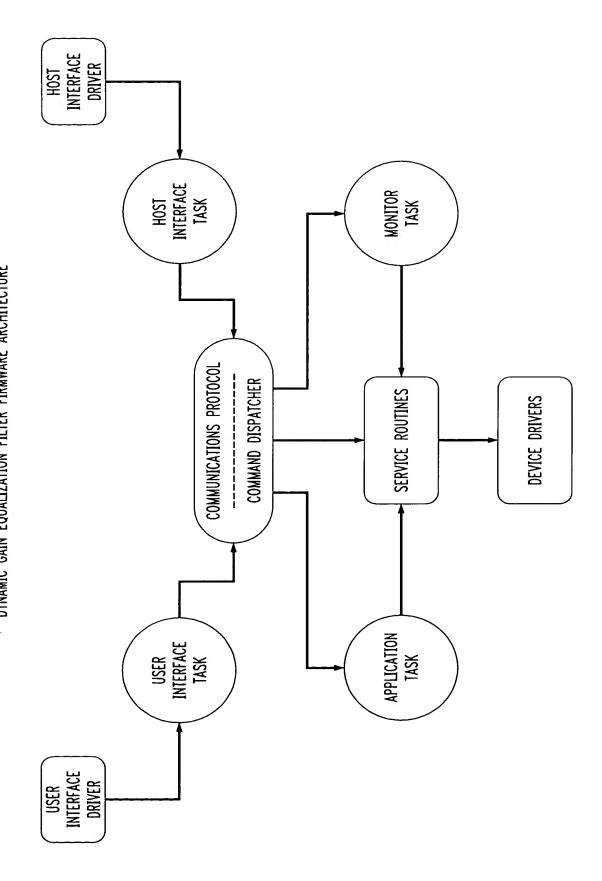
DYNAMIC GAIN EQUALIZATION FILTER POWER CONTROL STATE



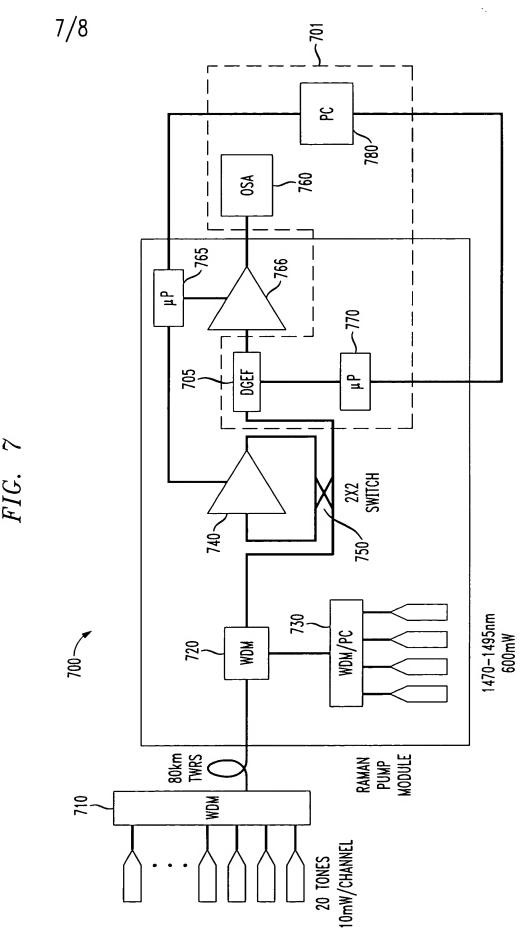


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FIG.  $egin{align*} FIG. & G \ \end{array}$  Dynamic gain equalization filter firmware architecture



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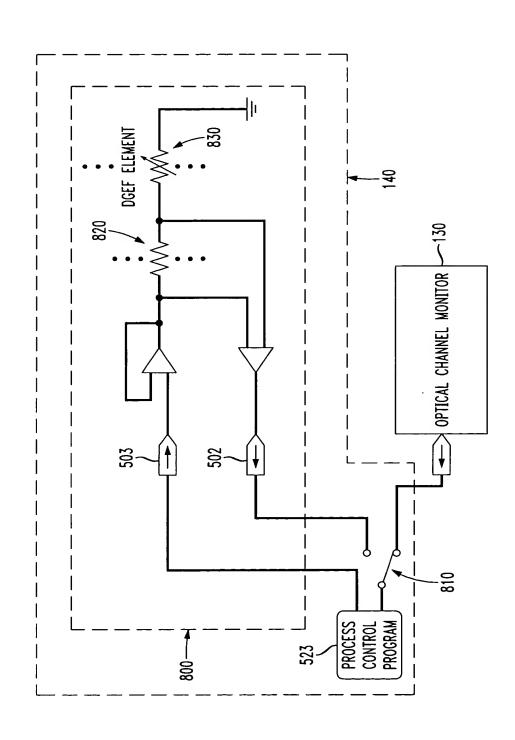


FIG. 8

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